

IN THE CLAIMS:

1. A processing system comprising:
a processor;
a volatile memory device coupled to communicate with the processor; and
a non-volatile memory device coupled to communicate with the processor and the volatile memory device, wherein the non-volatile memory device transfers data directly to the volatile memory device during power-up without control from the processor.
2. The processing system of claim 1 wherein the volatile memory device initiates the data transfer in response to a reset signal.
3. The processing system of claim 1 wherein the volatile memory device provides a system reset signal to the processor after the data is transferred from the non-volatile memory device.
4. The processing system of claim 1 wherein the processor is coupled to store data in the non-volatile memory device via a serial bus.
5. The processing system of claim 1 wherein the volatile memory device initiates the data transfer in response to a reset signal provided by an external reset controller.
6. A processing system comprising:
a processor;
a synchronous memory device coupled to communicate with the processor via a synchronous bus; and

a flash memory device coupled to communicate with the processor via a serial bus and communicate with the synchronous memory device via a direct bus, wherein the flash memory device transfers data directly to the synchronous memory device during power-up.

7. The processing system of claim 6 wherein the synchronous memory device initiates the data transfer in response to a reset signal provided by an external reset controller.

8. The processing system of claim 7 wherein the synchronous memory device provides a system reset signal to the processor after the data is transferred from the flash memory device.

9. The processing system of claim 6 wherein the synchronous memory device is an SDRAM.

10. The processing system of claim 6 wherein the synchronous memory device is an RDRAM.

11. A processor system power-up method comprising:
detecting a power-up condition and providing a reset signal to a synchronous memory;
initiating a direct data transfer from a non-volatile memory to the synchronous memory in response to the reset signal; and
providing a system reset signal from the synchronous memory to a processor.

12. The method of claim 11 wherein the synchronous memory device is an SDRAM.

20. A processor system power-up method comprising:
detecting a power-up condition with a reset controller and providing a reset signal to a rambus dynamic random access memory (RDRAM);
using the RDRAM, initiating a direct data transfer from a flash memory to the synchronous memory in response to the reset signal; and
providing a system reset signal from the RDRAM to a processor after the data has been transferred.
21. A data transfer method comprising:
initiating a direct data transfer from a non-volatile memory to a volatile storage device; and
transferring data from the non-volatile memory to the volatile storage device without control from an external processor.